



BUK9628-55A

N-channel TrenchMOS logic level FET

Rev. 02 — 17 February 2011

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

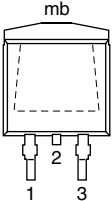
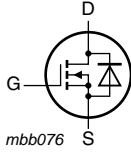
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	55	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3	-	-	42	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	99	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$	-	22	25	mΩ
		$V_{GS} = 4.5\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$	-	-	30	mΩ
		$V_{GS} = 5\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$; see Figure 12 ; see Figure 13	-	24	28	mΩ
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 34\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	-	57.8	mJ



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p style="text-align: center;">SOT404 (D2PAK)</p>	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

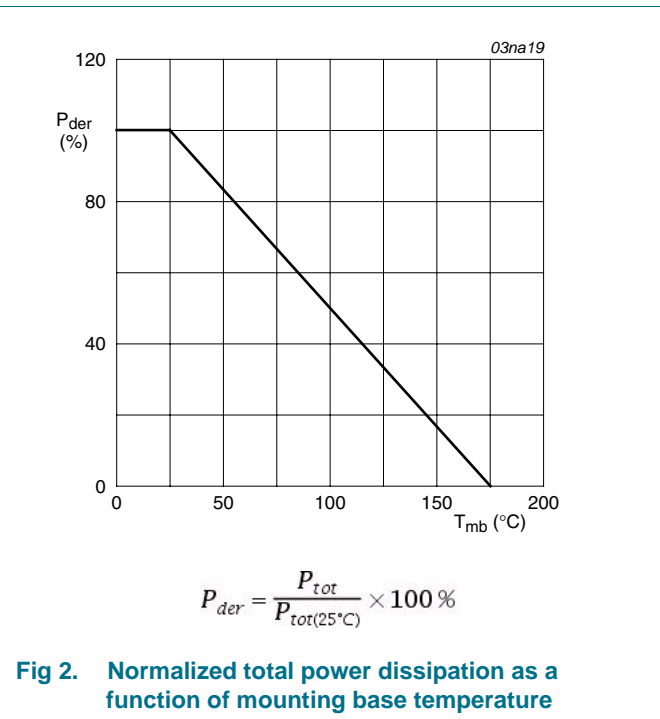
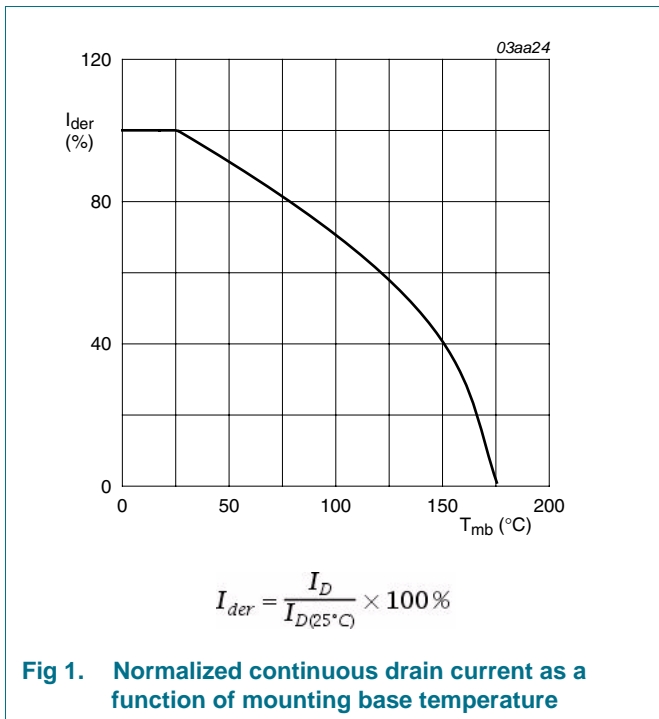
Type number	Package		Version
	Name	Description	
BUK9628-55A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	55	V
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	55	V
V _{GS}	gate-source voltage		-10	10	V
I _D	drain current	T _{mb} = 100 °C; V _{GS} = 5 V; see Figure 1	-	30	A
		T _{mb} = 25 °C; V _{GS} = 5 V; see Figure 1 ; see Figure 3	-	42	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; see Figure 3	-	168	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	99	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
V _{GSM}	peak gate-source voltage	pulsed; t _p ≤ 50 μs	-15	15	V
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	42	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	168	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 34 A; V _{sup} ≤ 55 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped	-	57.8	mJ



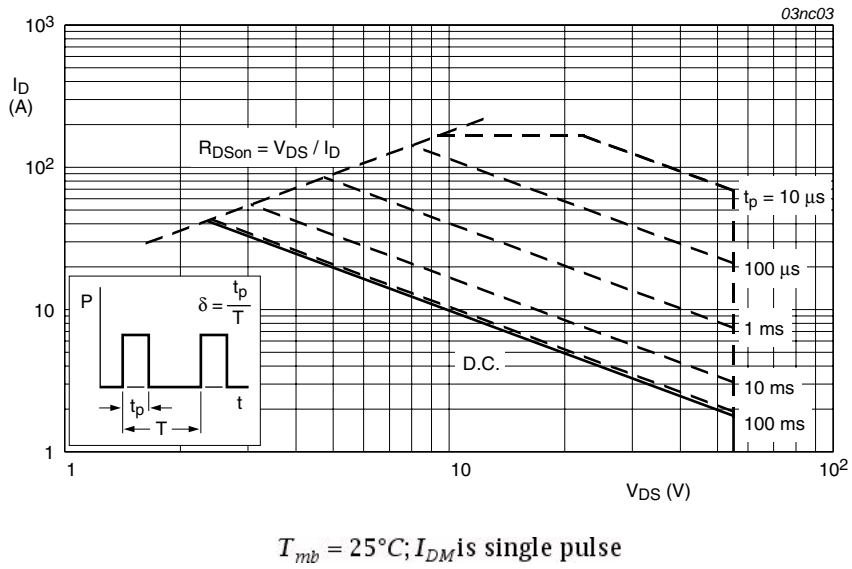


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board; minimum footprint	-	50	-	K/W

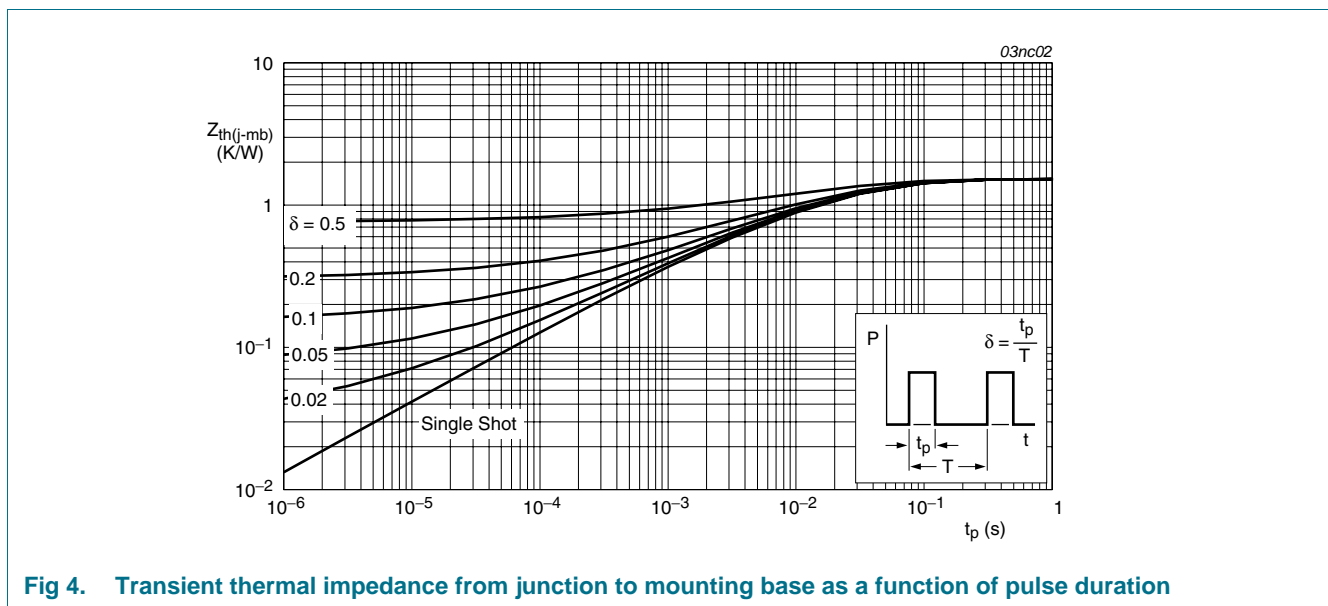
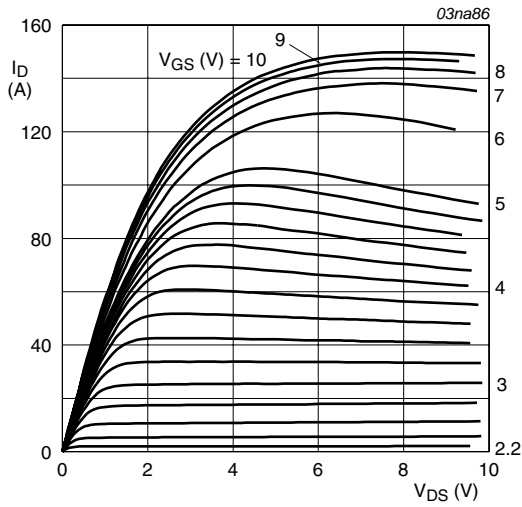


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

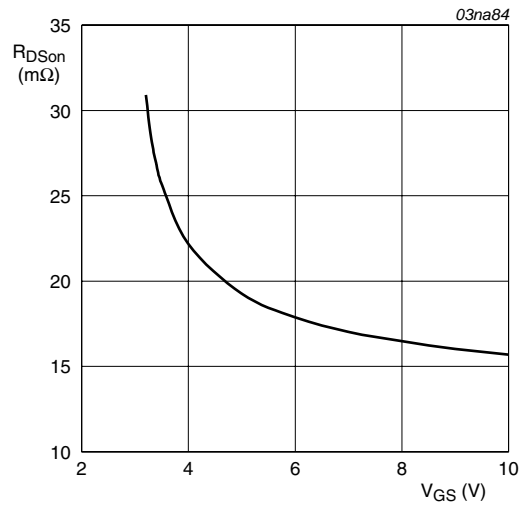
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 11	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 11	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 11	-	-	2.3	V
I_{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	μA
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13	-	-	56	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	22	25	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	-	30	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13	-	24	28	m Ω
Dynamic characteristics						
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 14	-	1200	1725	pF
C_{oss}	output capacitance		-	210	252	pF
C_{rss}	reverse transfer capacitance		-	140	195	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	14	-	ns
t_r	rise time		-	125	-	ns
$t_{d(off)}$	turn-off delay time		-	64	-	ns
t_f	fall time		-	68	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to centre of die ; $T_j = 25 \text{ }^\circ\text{C}$	-	2.5	-	nH
		from drain lead 6 mm from package to centre of die ; $T_j = 25 \text{ }^\circ\text{C}$	-	4.5	-	nH
L_S	internal source inductance	from source lead to source bond pad ; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s};$ $V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	35	-	ns
Q_r	recovered charge		-	70	-	nC



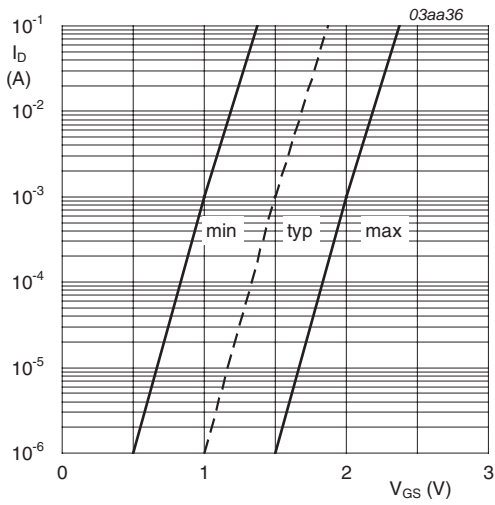
$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



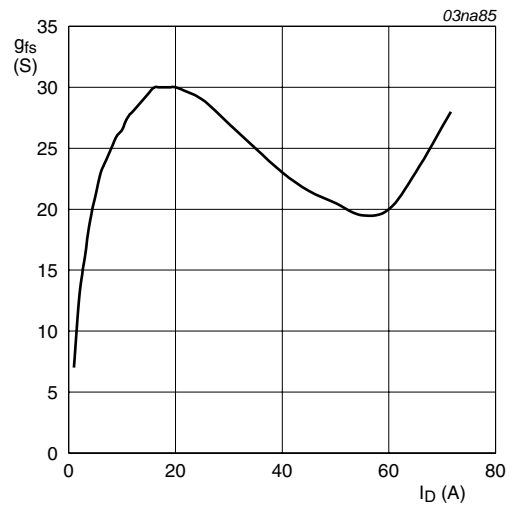
$T_j = 25^\circ\text{C}; I_D = 15\text{A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

Fig 8. Forward transconductance as a function of drain current; typical values

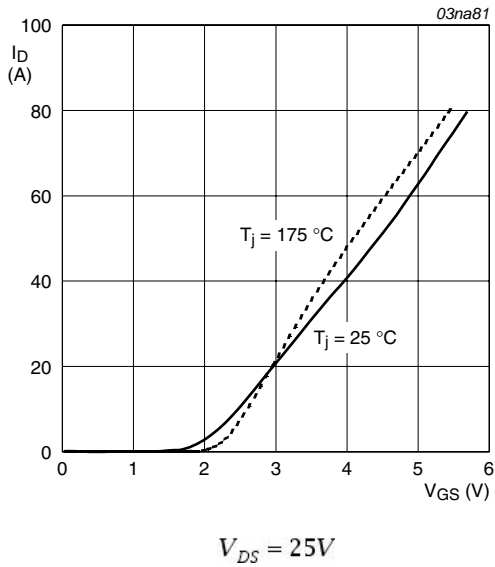


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

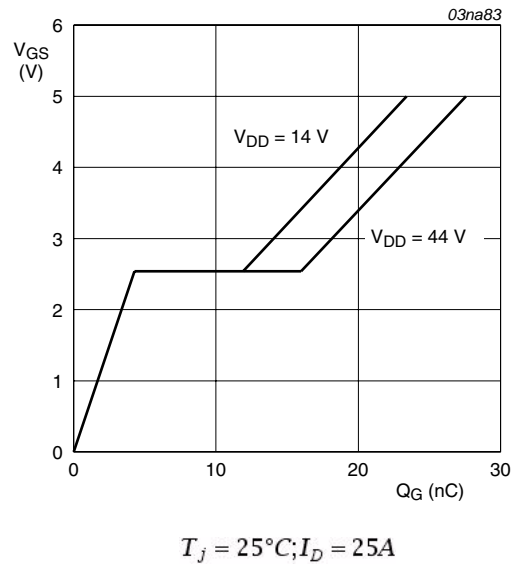


Fig 10. Gate-source voltage as a function of turn-on gate charge; typical values

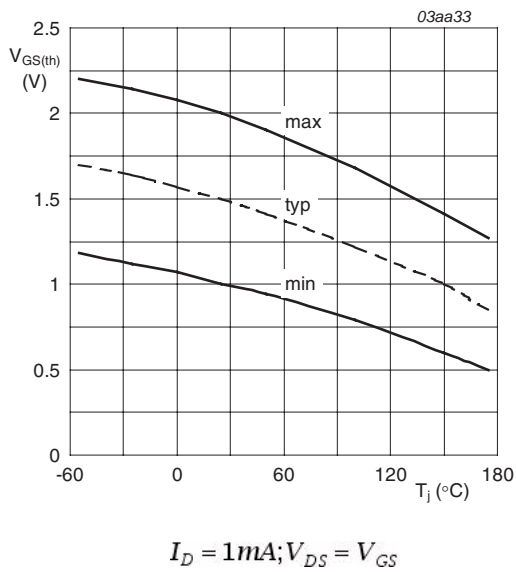


Fig 11. Gate-source threshold voltage as a function of junction temperature

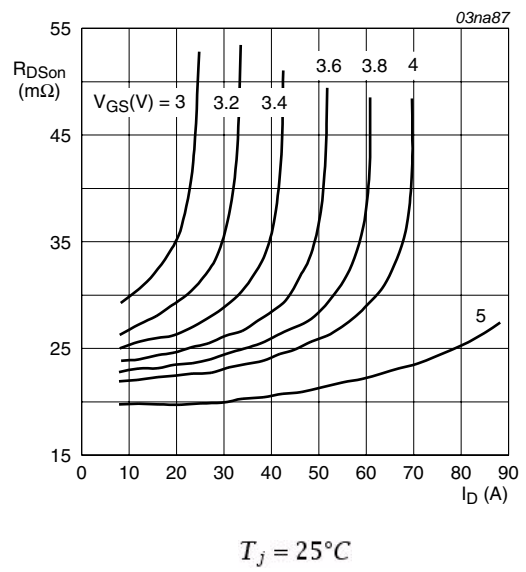
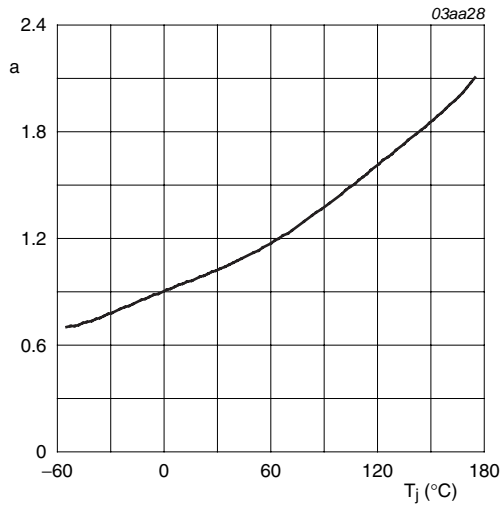
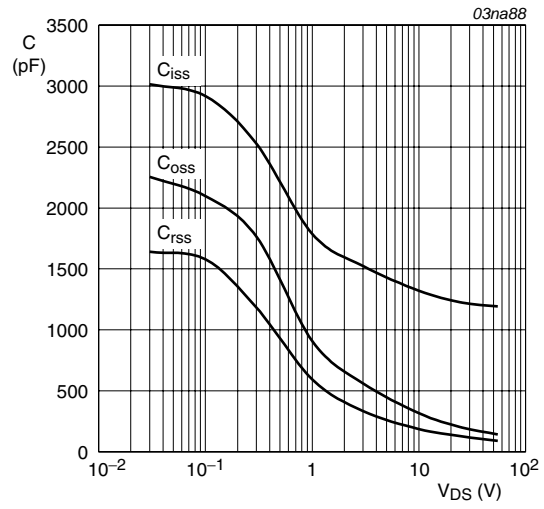


Fig 12. Drain-source on-state resistance as a function of drain current; typical values



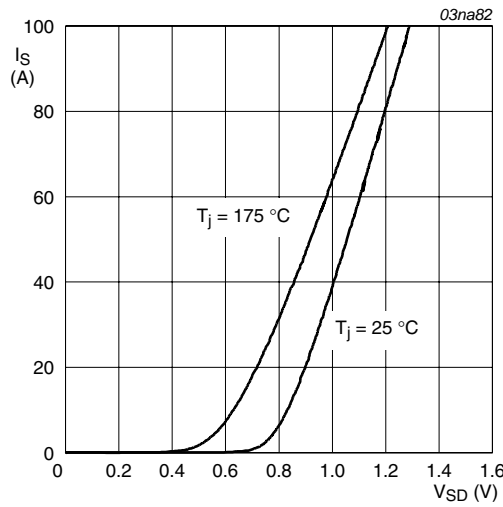
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



$V_{GS} = 0V; f = 1MHz$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



Fig 16. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9628-55A v.2	20110217	Product data sheet	-	BUK9528_9628_55A v.1
Modifications:				
				<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Type number BUK9628-55A separated from data sheet BUK9528_9628_55A v.1.
BUK9528_9628_55A v.1	20010118	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status ^[1] ^[2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 17 February 2011

Document identifier: BUK9628-55A